

WHAT IS CLAIMED IS:

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1. A circuit board comprising:
 - 2 a first conductive pad;
 - 3 a second conductive pad;
 - 4 a capacitive element connected between the first and the second conductive
 - 5 pads; and
 - 6 a series-resonant impedance coupled to the first pad, the series-resonant
 - 7 impedance comprising a serpentine conductor and a tuning
 - 8 capacitance.
 - 1 2. A circuit board as defined in Claim 1, wherein the serpentine
 - 2 conductor is formed from a conductor that is printed on the circuit board.
 - 1 3. A circuit board as defined in Claim 2, wherein tuning capacitance is
 - 2 planar in form.
 - 1 4. A circuit board as defined in Claim 3, wherein the tuning capacitance
 - 2 is printed on the circuit board.
 - 1 5. A circuit board as defined in Claim 1, wherein the serpentine
 - 2 conductor comprises:
 - 3 a plurality of substantially linear segments;
 - 4 an originating segment coupling a first linear segment to the first pad;
 - 5 a terminating segment coupling a second linear segment to the capacitance;
 - 6 and
 - 7 a turn coupling two adjacent linear segments.
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2 6. A circuit board as defined in Claim 1, wherein serpentine conductor
 - 3 comprises:
 - 3 at least one intermediate linear segment;
 - 4 a first turn coupling the originating segment to the first linear segment;

5 a second turn coupling the first linear segment to an intermediate linear
6 segment; and
7 a second turn coupling an intermediate linear segment to the second linear
8 segment.

1 7. A circuit board as defined in Claim 6, wherein the serpentine
2 conductor has a length (L) and a width (W) and wherein the respective lengths of the
3 turns establishes a space (S) between adjacent linear segment and wherein the number
4 of turns is equal to N, and wherein S, L, W and N are chosen so that the serpentine
5 conductor is at least approximately series resonant with the tuning capacitance at a
6 significant frequency F^0 .

1 8. A circuit board as defined in Claim 7, wherein the tuning capacitance
2 is substantially rectangular.

1 9. A circuit board as defined in Claim 8, wherein the linear segments are
2 respectively mutually parallel.

1 10. A computer system comprising:
2 a printed circuit board;
3 at least one integrated circuit device mounted on the printed circuit board, the
4 integrated circuit device having a significant frequency, F_0 ;
5 an active conductor coupled to the integrated circuit device;
6 a reference conductor coupled to the integrated circuit device;
7 a first pad coupled to the active conductor;
8 a second pad coupled to the reference conductor;
9 a capacitor coupled between the first pad and the second pad; and
10 means coupled to the capacitor for attenuating signals at F_0 , the means
11 comprising a serpentine conductor and a tuning capacitance.

1 11. A computer system as defined in Claim 10, wherein the reference
2 conductor provides a ground potential to the integrated circuit device.

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1 12. A computer system as defined in Claim 11, wherein the active
2 conductor supplies an operating voltage to the integrated circuit device.

1 13. A computer system as defined in Claim 11, wherein the active
2 conductor supplies an operating signal to the integrated circuit device.

1 14. A computer system as defined in Claim 10, wherein tuning capacitance
2 is printed on the circuit board in the form of a substantially rectangular plane.

1 15. A computer system as defined in Claim 14, wherein the tuning
2 capacitance is coupled to the reference conductor.

1 16. A computer system as defined in Claim 14, wherein the serpentine
2 conductor is printed on the printed circuit board.

1 17. A circuit board as defined in Claim 14, wherein the serpentine
2 conductor comprises:

3 a plurality of substantially linear segments;

4 an originating segment coupling a first linear segment to the first pad;

5 a terminating segment coupling a second linear segment to the capacitance;

6 and

7 a turn coupling two adjacent linear segment.

1 18. A circuit board as defined in Claim 17, wherein serpentine conductor
2 comprises:

3 at least one intermediate linear segment;

4 a first turn coupling the originating segment to the first linear segment;

5 a second turn coupling the first linear segment to an intermediate linear
6 segment; and

7 a second turn coupling an intermediate linear segment to the second linear
8 segment.

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24. A method as defined in Claim 23, wherein the inductance is deposited to form:

- at least one intermediate linear segment;
- a first turn coupling the originating segment to the first linear segment;
- a second turn coupling the first linear segment to an intermediate linear segment;
- a second turn coupling an intermediate trace to the second trace; and
- a third turn coupling an intermediate segment to the second trace.

25. A method as defined in Claim 24, wherein the inductance is deposited in a manner so that:

- (i) the inductance has a length (L) and a width (W);
- (ii) respective lengths of the turns establishes a space (S) between adjacent linear segments;
- (iii) the number of turns is equal to (N); and
- (iv) S, L, W, S and N establish a magnitude of the inductance such that the inductance is at least approximately series resonant with the tuning capacitance at F_0 .

26. A method as defined in Claim 23, wherein the tuning capacitance is formed by depositing a planar conductor on a first surface of the PCB and positioning the planar conductor in proximity with a ground plane.

27. A method as defined in Claim 26, wherein the inductance is deposited to form:

- at least one intermediate linear segment;
- a first turn coupling the originating segment to the first linear segment;
- a second turn coupling the first linear segment to an intermediate linear segment;
- a second turn coupling an intermediate linear segment to the second linear segment; and
- a third turn coupling an intermediate segment to the second linear segment.

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28. A method as defined in Claim 25, wherein the inductance is deposited in a manner so that:

- (i) the inductance has a length (L) and a width (W);
- (ii) respective lengths of the turns establishes a space (S) between adjacent linear traces;
- (iii) the number of turns is equal to (N); and

(iv) S, L, W, S and N establish a magnitude of the inductance such that the inductance is at least approximately series resonant with the tuning capacitance at F_0 .

29. In an electronic equipment, a circuit for attenuating spurious signals at high frequencies, the circuit comprising:

- a power pad;
- a reference pad;
- a discrete capacitor coupled between the power pad and the reference pad;
- a ground plane; and
- a printed circuit LC network connected to the power pad and coupled to the ground plane, and resonant at a predetermined frequency of a spurious signal, the LC network comprising:
 - a capacitive element;
 - a plurality of substantially linear segments;
 - an originating segment coupling a first linear segment to the power pad;
 - a terminating segment coupling a second linear segment to the capacitive element; and
 - a turn coupling two adjacent linear segments.

30. A circuit as defined in Claim 29, wherein the LC network further comprises:

- at least one intermediate linear segment;
- a first turn coupling the originating segment to the first linear segment;

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- 5 a second turn coupling the first linear segment to an intermediate linear
6 segment;
7 a second turn coupling an intermediate linear segment to the second linear
8 segment; and
9 a third turn coupling an intermediate segment to the second linear segment.

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contd. 1 31. A circuit as defined in Claim 29, wherein the capacitive element is
2 formed by affixing a planar conductor on a first surface of a printed circuit board in
3 proximity with the ground plane.

1 32. A circuit as defined in Claim 31, wherein the ground planes is affixed
2 to a second surface of the printed circuit board.

1 33. A circuit as defined in Claim 31, wherein the LC network further
2 comprises:
3 at least one intermediate linear segment;
4 a first turn coupling the originating segment to the first linear segment;
5 a second turn coupling the first linear segment to an intermediate linear
6 segment;
7 a second turn coupling an intermediate linear segment to the second linear
8 segment; and
9 a third turn coupling an intermediate segment to the second linear segment.

1 34. A circuit as defined in Claim 34, wherein the linear segments are
2 mutually substantially parallel.

1 35. A circuit as defined in Claim 33, wherein the printed circuit LC
2 network comprises a number, N, substantially linear segments, each having a width,
3 W, and mutually-spaced from an adjacent linear segment by a distance, S, where N,
4 W and S are chosen to form an inductance that in combination with the capacitive
5 element and the discrete capacitor effects substantial attenuation at the predetermined
6 frequency.

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1 36. In an electronic equipment, a circuit module comprising:
2 a printed circuit board having a top surface and a bottom surface;
3 a first conductive pad;
4 a second conductive pad;
5 a ground plane;
6 a capacitor coupled between the first and the second conductive pads; and
7 means, including an inductance and a capacitance, coupled to the first pad for
8 suppressing spurious signals at a predetermined frequency.

1 37. A circuit module as defined in claim 36, wherein the means consists
2 essentially of a conductive trace disposed on the printed circuit board.

1 38. A circuit module as defined in Claim 1, wherein the means comprises:
2 a plurality of substantially linear segments;
3 an originating segment coupling a first linear segment to the first pad;
4 a terminating segment coupling a second linear segment to the capacitance;
5 and
6 a turn coupling two adjacent linear segments.

1 39. A circuit module as defined in Claim 39, wherein the means
2 comprises:
3 at least one intermediate linear segment;
4 a first turn coupling the originating segment to the first linear segment;
5 a second turn coupling the first linear segment to an intermediate linear
6 segment; and
7 a third turn coupling an intermediate linear segment to the second linear
8 segment.